UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/704,156	11/01/2000	Takeshi Wakabayashi	00791/LH	3188

7590 07/31/2002

Holtz Goodman Langer & Chick PC
767 Third Avenue 25th Floor
New York, NY 10017-2023

EXAMINER
THAI, LUAN C

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/704,156	WAKABAYASHI, TAKESHI	
	Examiner	Art Unit	
	Luan Thai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 17-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 17-20,24-37 is/are rejected.

7)☒ Claim(s) 21-23 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office action is responsive to the amendment filed May 06, 2002.

Claims **1-16** have been canceled.

Newly added claims **17-37** are pending in this application.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17-18 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikazu (5,989,982 of record) in view of Elenius et al. (6,287,893).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 17-18, Yoshikazu teaches (figures 1-6, especially see figures 2A-2H and 3A-3H) a method manufacturing a semiconductor device comprising the steps of: preparing a semiconductor wafer 5 having an upper surface, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, a plurality of outer connection terminals 2 formed on the upper surface; adhering a dicing tape 7 to the semiconductor wafer before making trenches (figures 2B-2C and 3B-3C) in those parts of the wafer which lie between chip-forming regions thereof, each trench

extending through the thickness of the wafer from the upper surface; forming a seal film 12 on the upper surface of the wafer, filling the trenches and exposing the outer connection terminal 2 at one surface; cutting the seal film 12 along the trenches (figures 2G-2H and 3G-3H), removing those parts of the seal film which have a smaller width than the trenches; peeling the dicing tape 7 from the semiconductor wafer. Yoshikazu fails teach a seal film being formed on the lower surface of the semiconductor wafer.

Elenius et al while related to a similar chip-scale-package design teach an additional step of coating a protective layer (34) onto the rear surface of the semiconductor wafer 14 in order to provide mechanical protection to the backside of the die during handling (Col. 8, lines 29+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Elenius et al's teachings to Yoshikazu's method by performing the additional step of coating a protective layer onto the rear surface of the semiconductor wafer in order to provide mechanical protection to the backside of the die during handling.

3. Claims 19-20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikazu (5,989,982 of record) in view of Elenius et al. (6,287,893) and further in view of Sasaki et al. (5,888,883 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 19-20 and 24, the proposed method of Yoshikazu and Elenius et al. discloses all the limitations of the claimed invention as detailed above except for a

support tape adhered to the upper surface of the first seal film after the first seal film being cut (as recited in claim 19), and a step of polishing the lower surface of the semiconductor wafer to reduce a thickness of the semiconductor wafer (as recited in claims 20 and 24).

Sasaki et al. teach (Figures 8-23, especially see figures 8-10) a method for making a semiconductor device including a step of adhering a support tape 26 to an upper surface of the seal film after the seal film being cut in order to process the next step of polishing the lower surface of the semiconductor wafer, thereby reducing the thickness of the semiconductor wafer (Col. 6, lines 34+ and Col. 7, lines 1+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Sasaki et al.'s teachings to Yoshikazu's process in order to effectively perform the step of polishing the lower surface of the semiconductor wafer, thereby reducing the thickness of the semiconductor wafer.

4. Claims 25 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikazu (5,989,982 of record) in view of Elenius et al. (6,287,893) and further in view of Ohuchi (6,107,164).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 25 and 37, the proposed method of Yoshikazu and Elenius et al. discloses all the limitations of the claimed invention as detailed above except for a

step of polishing the upper surface of the first seal film until the top surface of each of the outer connection terminals to be exposed.

Ohuchi while related to a similar chip-scale-package design teaches (see specifically figures 3A-3D) a method comprising steps: forming a seal film 23 on the upper surface of the semiconductor wafer 10 so as to cover the top surface of each of the outer connection terminals 4, and wherein the upper surface of the seal film 23 is then polished until the top surface of each of the outer connection terminals to be exposed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Ohuchi's method to the proposed method of Yoshikazu and Elenius et al in order to form the seal film on the upper surface of the wafer without using the molding die (10).

5. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikazu (5,989,982 of record) in view of Elenius et al. (6,287,893) and further in view of Yamaji et al. (6,159,837 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 26-27, the proposed method of Yoshikazu and Elenius et al. discloses all the limitations of the claimed invention as detailed above except for the steps of forming wiring and electrodes on the upper surface of the wafer.

Yamaji et al while related to a similar chip-scale-package design teach (see specifically figures 1A-1C) a method comprising the steps: forming on the upper surface

of a semiconductor wafer 1 an insulating film 3 having openings to expose connection pads 2, forming on the insulating film 3 wirings 4 to connected to the connection pads 2, and forming pillar-shaped electrodes 7 on the wirings 4. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Yamaji et al's teachings to the proposed method of Yoshikazu and Elenius et al in order to form the wirings and the pillar-shaped electrodes for the chip-scale-package.

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikazu (5,989,982 of record) in view of Elenius et al. (6,287,893) and further in view of Yamaji et al. (6,159,837 of record) and Ohuchi (6,107,164).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 28, the proposed method of Yoshikazu, Elenius et al and Yamaji et al discloses all the limitations of the claimed invention as detailed above except for a step of polishing the upper surface of the first seal film until the top surface of each of the outer connection terminals to be exposed.

Ohuchi while related to a similar chip-scale-package design teaches (see specifically figures 3A-3D) a method comprising steps: forming a seal film 23 on the upper surface of the semiconductor wafer 10 so as to cover the top surface of each of the outer connection terminals 4, and wherein the upper surface of the seal film 23 is then polished until the top surface of each of the outer connection terminals to be exposed. It would have been obvious to one of ordinary skill in the art at the time the

invention was made to apply Ohuchi's method to the proposed method of Yoshikazu, Elenius et al and Yamaji et al in order to form the seal film on the upper surface of the wafer without using the molding die (10).

7. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikazu (5,989,982 of record) in view of Ohuchi (6,107,164).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 29, Yoshikazu teaches (figures 1-6, especially see figures 2A-2H and 3A-3H) a method manufacturing a semiconductor device comprising the steps of: preparing a semiconductor wafer 5 having an upper surface, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, a plurality of outer connection terminals 2 formed on the upper surface; adhering a dicing tape 7 to the semiconductor wafer before making trenches (figures 2B-2C and 3B-3C) in those parts of the wafer which lie between chip-forming regions thereof, each trench extending to the dicing tape 7 in part through the thickness of the wafer from the upper surface of the wafer; forming a seal film 12 on the upper surface of the wafer, filling the trenches and exposing the outer connection terminal 2 at one surface; cutting the seal film 12 along the trenches (figures 2G-2H and 3G-3H), removing those parts of the seal film which have a smaller width than the trenches; peeling the dicing tape 7 from the

semiconductor wafer. Yoshikazu fails teach a seal film being formed on the lower surface of the semiconductor wafer.

Ohuchi while related to a similar chip-scale-package design teaches (see specifically figures 3A-3D) a method comprising steps: forming a seal film 23 on the upper surface of the semiconductor wafer 10 so as to cover the top surface of each of the outer connection terminals 4, and wherein the upper surface of the seal film 23 is then polished until the top surface of each of the outer connection terminals to be exposed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Ohuchi's teachings to Yoshikazu's method in order to form the seal film on the upper surface of the wafer without using the molding die (10).

Regarding claim 30, although Yoshikazu does not explicitly teach a full thickness of the dicing tape not being cut, this feature is taken to be inherent in the process of Yoshikazu, since a means of cutting the wafer into individual chips and a means of the pealing of the dicing tape are disclose, and it is apparent that a full thickness of the dicing tape 7 is not cut for easier to be peeled off.

8. Claims 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikazu (5,989,982 of record) in view of Ohuchi (6,107,164) and further in view of Sasaki et al. (5,888,883 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 31-34, the proposed method of Yoshikazu and Ohuchi discloses all the limitations of the claimed invention as detailed above except for a support tape adhered to the upper surface of the first seal film after the first seal film being cut (as recited in claim 31) and polishing the lower surface of the semiconductor.

Sasaki et al. teach (Figures 8-23, especially see figures 8-10) a method for making a semiconductor device including a step of adhering a support tape 26 to an upper surface of the seal film after the seal film being cut in order to process the next step of polishing the lower surface of the semiconductor wafer, thereby reducing the thickness of the semiconductor wafer (Col. 6, lines 34+ and Col. 7, lines 1+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Sasaki et al.'s teachings to the proposed method of Yoshikazu and Ohuchi in order to effectively perform the step of polishing the lower surface of the semiconductor wafer, thereby reducing the thickness of the semiconductor wafer.

Allowable Subject Matter

9. Claims 21-23 are (is) objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is an examiner's statement of reasons for allowance: the prior art fails to teach the trenches being formed so as to cut the semiconductor wafer completely in a thickness direction and to form concavities in an upper portion of the dicing tape.

Conclusion

11. Applicant's arguments with respect to newly added claims **17-20 and 24-37** have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the newly added claims 17-37 raise new issues that would require further consideration and/or search. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for

the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai
July 17, 2002

KAMAND CUNEO
PRIMARY EXAMINER